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**Patent Application for**

**An Improved MOS Varactor For LC VCOs**

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## An Improved MOS Varactor For LC VCOs

### Field of the Invention

[0001] The invention generally relates to voltage controlled oscillators for radio frequency circuits, and specifically to an MOS varactor for such circuits.

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### Background Art

[0002] Implementing monolithic voltage controlled oscillators (VCOs) in standard complementary metal oxide semiconductor (CMOS) technology is a major challenge for the design of radio-frequency (RF) CMOS transceiver integrated circuits (ICs). Recent work has shown that MOS devices for voltage control can produce better VCO performance than commonly used diode varactors. These advantages include better tuning range, better Q, and so better VCO phase noise. Both nMOS and pMOS variety devices can be used as varactors, typically with source and drain terminals shorted ( $S=D$ ), and a tuning voltage applied to the gate terminal with respect to the source and drain.

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[0003] Several modes of MOS varactor operation are known depending on the connection of the fourth device terminal, the transistor back gate (BG). For standard bulk p-type substrate CMOS technology, only pMOS devices can be used since the back gate BG of nMOS devices are tied to a grounded substrate. New triple well CMOS technologies, now common in 0.18 and 0.13  $\mu\text{m}$  gate lengths, offer a triple well option that extends the flexibility of BG terminal connection for an nMOS device. nMOS devices have advantages over pMOS devices as varactors in terms of better Q and better capacitance range.

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[0004] When used in a VCO, MOS varactors typically operate under large signal tank swings necessary for good phase noise and moderate gain constant ( $K_{vco}$ ) or tuning gain (Hz/V). These large signals, typically 1 to 8 volts peak-to-peak over a back to back, series connected, pair of varactors, are well known to linearize the sharp capacitance variation with tuning voltage ( $C(V)$ ) which typically varies from  $C_{min}$  to  $C_{max}$  in a few hundred mV under small signal conditions.

[0005] Three MOS varactor modes of operation are recognized. In the first mode (Mode 1), the pMOS BG is tied to the drain supply voltage  $V_{DD}$ , or the nMOS substrate is grounded, or a triple well nMOS BG is tied to ground. This mode ( $S=D$ ,  $BG=GND$  as nMOS) has superior  $C(V)$  range, using the inversion MOS bias region of operation only. For this reason, it is called I-MOS for inversion MOS. One disadvantage of this mode with supply referenced VCO tanks and/or tuning voltages is a sensitivity to supply noise and supply variations (frequency pushing). This deficiency often requires a remedy of additional supply regulation and/or large off-chip capacitor filtering that are undesirable for low power and low cost communication applications.

[0006] The second MOS varactor mode (Mode 2) ties the pMOS or triple well nMOS back gate BG to the source and drain. This mode ( $S=D=BG$ ) has a reduced  $C(V)$  range, and uses both inversion and accumulation MOS bias regions of operation. It is not sensitive to supply noise or frequency pushing because its BG is isolated from both supply and ground. But, under typical large signal VCO swing operation it has less than half the tuning range, which makes it less advantageous to use.

[0007] Standard CMOS technologies have process and temperature variations that

must be tuned out by the VCO. Also, many communication applications (such as Sonet OC-192) have multiple rates or frequencies that must be tuned to (9.954, 10.66, 11.1 GHz for OC-192). Both requirements make a large VCO tuning range or large varactor C(V) range important. Even for implementations that use other  
5 methods for tuning to rate or tuning out process variations (for example, multiple switched VCOs and discreet tuning methods such as switched capacitors or inductors), frequency variations from temperature affects alone still make a large varactor C(V) range important because these alternative tuning methods present their own capacitance load to the VCO tank, there by decoupling or attenuating  
10 the C(V) affect of the varactor alone.

[0008] The third MOS varactor mode (Mode 3) is an accumulation-only device called an A-MOS device. It is formed by removing source and drain diffusions (p+ type for a pMOS device), and perhaps adding bulk contacts (n+ type for what was  
15 a pMOS device). The resulting device has a floating BG and is not strictly a MOS transistor device. The A-MOS floating BG makes it insensitive to supply noise/pushing in a VCO application. While the A-MOS C(V) range is typically as large as an I-MOS even under large signal operation, it suffers from the disadvantage of not being a commonly used, well-modeled CMOS device  
20 structure such as the standard nMOS or pMOS devices. As a result, the A-MOS device often is not well-controlled, reliably fabricated, or accurately modeled.

### Summary of the Invention

[0009] Embodiments of the present invention are directed to a varactor for CMOS  
25 technologies that has the advantages the I-MOS device, a large C(V) range, good Q, well-modeled and controlled in a standard process, but doesn't have its disadvantages, such as poor supply pushing and supply noise isolation.

[0010] Specific embodiments include a metal oxide semiconductor (MOS) varactor device having a source and a drain connected to each other, and a back gate, electrically separate from the source and drain, which is connected to a circuit common mode point. The common mode point may be referenced to a circuit supply voltage. The device may be part of a voltage controlled oscillator (VCO), for example, part of an LC tank circuit. The device may be an nMOS or a pMOS device.

#### Brief Description of the Drawings

[0011] Figure 1 shows an nMOS VCO with nMOS varactor having BG connected to a common mode point according to an embodiment of the present invention.

[0012] Figure 2 shows a pMOS VCO with pMOS varactor having BG connected to a common mode point.

[0013] Figure 3 shows a CMOS VCO with nMOS varactor having BG connected to a common mode point according to an embodiment of the present invention.

[0014] Figure 4 shows a CMOS VCO with pMOS varactor having BG connected to a common mode point.

[0015] Figure 5 shows an nMOS VCO with nMOS varactor having BG connected to an alternative common mode point.

[0016] Figure 6 shows a Mode 1 nMOS varactor resonant tank circuit with BG tied to ground.

[0017] Figure 7 shows  $F(V)$  and  $C(V)$  curves for a Mode 1 varactor circuit according to Figure 6.

[0018] Figure 8 shows a Mode 2 nMOS varactor resonant tank circuit with BG tied to the source and drain.

[0019] Figure 9 shows  $F(V)$  and  $C(V)$  curves for a Mode 2 varactor circuit according to Figure 8.

[0020] Figure 10 shows a Mode 4a nMOS varactor resonant tank circuit with BG tied to a  $V_{DD}$ -referred common mode point voltage according to an embodiment of the present invention.

[0021] Figure 11 shows  $F(V)$  and  $C(V)$  curves for a Mode 4a varactor circuit according to Figure 10.

[0022] Figure 12 shows a Mode 4b nMOS varactor resonant tank circuit with BG tied to a  $V_{DD}$ -referred common mode point voltage according to an embodiment of the present invention.

[0023] Figure 13 shows  $F(V)$  and  $C(V)$  curves for a Mode 4b varactor circuit according to Figure 12.

[0024] Figure 14 shows a Mode 1 varactor VCO schematic.

[0025] Figure 15 shows a Mode 2 varactor VCO schematic.

[0026] Figure 16 shows a Mode 4a varactor VCO schematic according to an embodiment of the present invention.

[0027] Figure 17 shows simulated VCO frequency pushing in a Mode 1 varactor VCO according to Figure 14.

[0028] Figure 18 shows simulated VCO frequency pushing in a Mode 2 varactor VCO circuit according to Figure 15.

[0029] Figure 19 shows simulated frequency pushing in a Mode 4a varactor VCO circuit according to claim 16.

[0030] Figure 20 shows a Mode 4a varactor VCO schematic with ground BG negative Gm devices.

[0031] Figure 21 shows simulated frequency pushing in a Mode 4a varactor VCO circuit according to Figure 20.

#### Detailed Description of Specific Embodiments

[0032] An improved MOS varactor for LC-tank VCO applications is formed by connecting the MOS varactor fourth terminal BG to a ground-isolated common mode point of the negative transconductance (Gm) devices used to pump the VCO tank, as shown in Figure 1, which shows a  $V_{DD}$ -referred tank, nMOS negative Gm device, cross-coupled differential VCO in a triple well CMOS process. This new varactor mode is referred to as the fourth mode (Mode 4). Since the tuning voltage and the common mode point are both  $V_{DD}$ -referred, supply noise is not coupled into the tank by the varactor back gate capacitance and the

VCO has excellent supply pushing (5 MHz/V simulated for this 10 GHz VCO example, or 90ppm for a +/- 5% 1.8V supply variation). For this example, the common mode point is held constant, at a  $V_{gs}$  from MN1, MN2 below  $V_{DD}$  by the current source, MN0. (An automatic leveling control is used to adjust the current  
 5 in the current source, MN0, to maintain a constant large signal tank swing across nMOS varactors, MN3 and MN4, thereby producing a constant common mode point from a constant current into a constant tank resonate impedance.)

[0033] Embodiments are also applicable to pMOS varactors and ground  
 10 referenced tanks. Such applications basically flip the circuit as shown in Figure 2, replacing nMOS with pMOS devices.

[0034] Embodiments also include a complementary CMOS VCO that has both nMOS and pMOS cross-coupled negative Gm devices pumping the LC tank  
 15 shown in Figure 3. The tuning voltage is  $V_{DD}$ -referred by the gate-source voltage  $V_{gs}$  of the pMOS negative Gm devices, MP1 and MP2. The common mode point also is  $V_{DD}$ -referred by the  $V_{gs}$  of the same pMOS devices, MP1 and MP2, in series with the  $V_{gs}$  of the nMOS negative Gm devices, MN1 and MN2. Since the tuning voltage and common mode point are both  $V_{DD}$ -referred, supply noise is not  
 20 coupled into the LC tank by the varactor BG capacitance, and the VCO has excellent supply pushing.

[0035] Embodiments also include a ground-referenced CMOS VCO that has a pMOS current source and pMOS varactors as shown in Figure 4.

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[0036] The common mode point located beneath a cross-coupled negative Gm pair and above a current source, provides a convenient connection to the varactor BG



that enhances the performance of the varactor in this type of VCO by eliminating supply pushing and supply noise coupling to the tank while still obtaining nearly the full  $C(V)$  inversion mode range from the varactor. One such convenience is that the node already exists in the differential circuit. However, it is also possible to implement embodiments of the invention by creating a separate common mode node as shown in Figure 5, where a mirrored current is dropped across a resistor from current source MN5 to  $V_{DD}$ , creating an alternative common mode point to connect an nMOS varactor BG. The voltage need not be dropped across a resistor, but some other device such as a diode or diode-connected MOS device, for example, can be used instead. Such an embodiment possesses beneficial supply noise, pushing suppression and full  $C(V)$  inversion mode range such as in an inherent common mode node. It is also possible for such embodiments to take the forms illustrated in the pMOS and CMOS versions with the inherent common node.

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#### *MOS Varactor Modes and Simulations*

[0037] Simulations of the small signal performance of the various MOS varactor modes can provide further insight. The BG of the nMOS varactors in Figure 6 is connected to ground as an inversion mode (I-MOS) MOS varactor in a simulation of a  $V_{DD}$ -referenced tank with dual nMOS varactors (MN0 and MN8), ideal inductor ( $L_0$ ), and an ideal capacitor ( $C_0$ ). Varactor sizes, capacitance ( $C_0=500\text{fF}$ ) and inductance ( $L_0=0.36\text{nH}$ ) values are chosen for a convenient resonance near 10 GHz. The relatively large fixed  $C_0$  capacitance also limits the tuning bandwidth of the varactors in a manner to be expected from an actual VCO with additional methods of tuning (such as switched MIMCAPs) and other sources of parasitic capacitance (from spiral inductors, negative GM devices, etc.). In a practical VCO, the tank of Figure 6 would require a source of energy such as that provided by the

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negative Gm transistors in a differential cross-coupled VCO.

[0038] For the purpose of this simulation, a 1 amp AC current source is applied across the tank, serving to generate an AC voltage at node "vout" that is equal to the tank impedance,  $Z_{\text{tank}}$ . As the frequency of this AC source is swept, a peaked impedance resonance waveform at vout is produced. The peak vout or highest impedance Z occurs at the tank resonant frequency,  $F_0$ , the frequency at which a corresponding VCO would oscillate. Tank Q is extracted from the swept waveform as the peak frequency divided by peak width at 1/2 peak value. Since the circuit has ideal inductance (L) and capacitance (C) components, the tank Q is completely determined by the varactor. A voltage source is applied to node "vtx" = D = S of the nMOS varactor to provide the varactor tuning voltage. By stepping this tuning voltage and sweeping the frequency of an AC simulation at each step, a set of frequency and Q vs tuning voltage and varactor C(V) curves can be constructed. The varactor C(V) is obtained from the BSIM3 MOS model and is the sum of the gate-source capacitance  $C_{gs}$ , gate-drain capacitance  $C_{gd}$ , and gate-back gate capacitance  $C_{gb}$  aspects that are generated by a DC simulation at each tuning voltage step.

#### 20 *Mode 1: I-MOS Varactor*

[0039] Figure 7 shows the simulated frequency and varactor capacitance vs. tuning voltage (x-axis labeled "vin"). Frequency change is monotonic with tuning voltage, relatively abrupt from 0.8 to 1 V with a total tuning range of 7.76 to 10.45 GHz and a 2690 MHz bandwidth (BW). In the lower half of Figure 7,  $C_{gs}$ ,  $C_{gd}$  and  $C_{gb}$  are plotted along with the sum of  $C_{gs}$  and  $C_{gd}$  (labeled cgs\_gd) and the total varactor C(V) (labeled cg\_tot).  $C_{gs}$  and  $C_{gd}$  are approximately equal and are the dominant varying capacitances for the I-MOS mode.  $C_{gb}$  rises somewhat as  $V_{gs}$

drops below  $V_{th}$  and limits the  $C(V)$  ratio  $C_{max}/C_{min}$  to 3.4 (340fF/100fF). The I-MOS  $Q$  (curve not shown) varies from 136 to 915. Under large signal operation, the abruptness of the  $C(V)$  transition is moderated by a time averaging of the varying capacitance, but the large constant  $C_{max}$  (and to some extent  $C_{min}$ ) region preserve a  
 5 large tuning bandwidth.

*Mode 2: D=S=BG Varactor*

[0040] Figure 8 shows an identical LC resonant circuit, except now the nMOS varactor has its back gate BG connected to its source and drain nodes ( $=S=D$ ). The  
 10 simulated tuning response of this circuit is shown in Figure 9. Some differences between this varactor mode and the previous I-MOS are apparent. The S-shaped frequency tuning ( $F(V)$ ) and  $C(V)$  curves of the I-MOS are replaced by U-shaped curves. The frequency change is not monotonic with tuning voltage, but is still abrupt for the inversion operation. An accumulation mode (tuning voltage from -  
 15 2.0 to +0.45V) is now evident and has approximately the same frequency range, 9.17 to 10.64 GHz, a 1468 MHz BW as the inversion mode, but in comparison to the I-MOS, the D=S=BG varactor has 55% the tuning bandwidth. The  $C(V)$  curves show a large rising  $C_{bg}$  at negative  $V_{gs}$  and a  $C_{max}/C_{min}$  ratio of 2.6 (340fF/130fF) that is approximately equal in both inversion and accumulation modes. The D=S=BG  
 20  $Q$  (curve not shown) varies from 82 to 380, less than the I-MOS varactor, but still relatively large compared to typical IC spiral inductor  $Q$ s.

[0041] A large signal bandwidth and capacitance ratio comparison of the D=S=BG varactor versus the I-MOS varactor produces an additional degradation caused by  
 25 the non-monotonic behavior of the  $C(V)$  in the accumulation region. For example this worsens the large signal tuning bandwidth to about 50% of that available from the I-MOS varactor when a 3Vpk-pk tank swing is time averaged over the U-

shaped  $C(V)$  response of a back to back, series connected, pair of such varactors. The larger the signal, the greater the BW reduction.

*Mode 4:  $D=S$ ,  $BG=CM$  Varactor*

5 [0042] Figure 10 shows another version of the LC resonant circuit, except now the nMOS varactor back gate BG is connected by a voltage source to the  $V_{DD}$  node according to one embodiment of the present invention. A 10K resistor in series with this voltage source and a 2.5pF cap from the common mode CM to circuit ground GND are added as a filter to further improve the tuning range of this

10 mode, but they are not fundamentally required as will be shown. This voltage source represents the voltage drop from  $V_{DD}$  resulting from one of the methods used to generate the common mode voltage as previously discussed. For the simulated  $F(V)$  and  $C(V)$  curves in Figure 11, this voltage is set to  $V_{dd}-1.3V$ , leaving 0.5V headroom for the current source when  $V_{DD}$  is 1.8V. At first glance,

15 the simulated performance of the  $BG=CM$  appears closest to the I-MOS varactor mode, with S-shaped  $F(V)$  and  $C(V)$  curves. Frequency change is monotonic with tuning voltage from -2.0 to 1.3V, relatively abrupt from 0.7 to 0.9 V with a total tuning range of 7.93 to 10.44 GHz, a 2518 MHz BW. This BW is only marginally less than the I-MOS varactor mode and nearly double that of the  $D=S=BG$  mode.

20 As with the I-MOS mode, in this mode  $C_{gb}$  rises somewhat as  $V_{gs}$  drops below  $V_{th}$  and limits the  $C(V)$  ratio  $C_{max}/C_{min}$  to 3.2 (340fF/107fF). The I-MOS Q (curve not shown) varies from 73 to 100 and although limited by the BG bias network is still substantially larger than necessary for realistic IC VCO tanks. Under large signal operation, the abruptness of the  $C(V)$  transition is moderated by a time averaging

25 of the varying capacitance, but the large constant  $C_{max}$  (and to some extent  $C_{min}$ ) region preserve a large tuning BW to a much greater extent than the U-shaped response of the  $D=S=BG$  varactor mode.

[0043] The effect of the filter capacitance  $C_{\text{filter}}$  can be seen in a simulation of an LC resonant circuit shown in Figure 12 that removes it. As shown in Figure 13, the  $F(V)$  and  $C(V)$  curves show an S-shaped characteristic, have less BW than those with  $C_{\text{filter}}$  (1912 vs 2518 MHz), but 600 MHz higher frequency and larger BW than the U-shaped D=S=BG varactor mode (1912 vs 1469 MHz). The  $C(V)$  curves look identical. Under large signal operation, the BW improvement of this mode without  $C_{\text{filter}}$  will retain more advantage over the D=S=BG mode because of the U-shaped  $C(V)$  affects already noted.

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#### *VCO Supply Pushing Simulations vs Varactor Mode*

[0044] Some benefits of embodiments of the invention can be seen when considering the supply pushing characteristics of VCOs constructed from mode 1 (I-MOS), mode 2 (D=S=BG) and mode 4a (embodiments of the invention, BG=CM, with  $C_{\text{filter}}$ ) varactors. Figures 14, 15, and 16 show simplified schematics of the mode 1, 2 and 4a VCOs considered. The top curves of Figures 17, 18, and 19 show the simulated response of these VCOs to a sixteen equal step variation in  $V_{\text{DD}}$  from 1.62 to 1.98V (+/- 10% of 1.8V). The supply pushing is the change in frequency with supply voltage, which is 450 MHz/V for mode 1 VCO, -10.6 MHz/V for mode 2 VCO and less than 4.9 MHz/V for mode 4a VCO, where the precision of the simulation result is generating numerical noise that prevents an even lower result from being observed. From these results, a 42x to 92x improvement in supply pushing can be seen for modes 2 and 4a over mode 1. Also considering the tuning range performance of these varactor modes from the other simulations above, further suggests benefits of embodiments of the invention over other MOS varactor modes. This is summarized in Table 1 below, along with a figure of merit that is the calculated small signal varactor BW/VCO pushing.

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**TABLE 1. Small Signal Varactor BW and VCO Pushing Summary for Modes 1,2,4a MOS varactors and VCOs**

Varactor/VCO	Varactor Small Signal Tuning BW (MHz)	VCO Supply Pushing (MHz/V)	Small Signal Varactor BW/VCO Pushing FOM
mode 1	2690	450	6
mode 2	1469	10.6	139
mode 4a	2519	4.9	514

[0045] In all of the VCOs discussed so far, the back gates of the negative transconductance devices are connected to their source terminals, except for those of the mode 1 VCO in Figure 14, where all the back gates are connected to ground.

- 5 The contribution of the transconductance ( $G_m$ ) devices to the overall pushing response of mode 1 can be calculated by analyzing the VCO in Figure 20, where the varactor is configured as in mode 4a, but the  $G_m$  back gates are connected to ground. Figure 21 shows the simulated pushing response of this VCO, 133 MHz/V (or about 1/3 of the total mode 1 performance), indicating the importance of an
- 10 appropriate negative  $G_m$  device BG connection for all of the Varactor modes.

#### *VCO Frequency, BW Simulations vs Varactor Mode*

- [0046] The large signal simulations of Figures 14, 15, and 16 further shows evidence of the advantage of various embodiments. For a now fixed  $V_{dd}$  supply,
- 15 the  $V_{tune}$  of each VCO is varied by 600mV and the tank swing held large at 2.5Vpk-pk differential. The difference in frequency for this  $V_{tune}$  variation is the VCO large signal tuning bandwidth. Table 2 below summarizes three simulated varactor tuning bandwidths and the calculated large signal VCO BW/pushing figure of merit.

**TABLE 2. Large Signal VCO BW and Supply Pushing Summary for Modes 1,2,4a VCOs**

VCO Varactor	VCO Large Signal Tuning BW (MHz)	VCO Supply Pushing (MHz/V)	Large Signal VCO BW/Pushing FOM
mode 1	718	450	1.6
mode 2	358	10.6	34
mode 4a	605	4.9	123

[0047] Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes  
5 and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention.